WHAT IS CLAIMED IS:

1. An EEPROM semiconductor device comprising:

(a) a plurality of field insulating films each extending perpendicularly to word lines;

(b) a plurality of memory cells arranged in a matrix, each memory cell including a floating gate, a control gate formed on said floating gate and doubling as a word line, and source and drain regions located at either sides of said control gate;

(c) a common source line extending in parallel with said word lines and connecting source regions of said memory cells with each other; and

(d) a first bit line extending perpendicularly to said word lines and connecting drain regions of said memory cells with each other.

2. The EEPROM semiconductor device as set forth in claim 1, wherein said common source line is constituted of a first metal wiring layer.

3. The EEPROM semiconductor device as set forth in claim 2, wherein said first metal wiring layer is composed of aluminum.

4. The EEPROM semiconductor device as set forth in claim 1, wherein said bit line is constituted of a second metal wiring layer.

5. The EEPROM semiconductor device as set forth in claim 4, wherein said second metal wiring layer is composed of aluminum.

6. The EEPROM semiconductor device as set forth in claim 1, further comprising a plurality of second bit lines formed above said drain regions of said memory cells, and wherein said first bit line connects said second bit lines with

one another.

7. The EEPROM semiconductor device as set forth in claim 6, wherein both said second bit lines and said common source line are constituted of a first metal wiring layer.

8. The EEPROM semiconductor device as set forth in claim 7, wherein said first metal wiring layer is composed of aluminum.

9. The EEPROM semiconductor device as set forth in claim 1, further comprising CMOS logic circuit including both said common source line and said first bit line, and formed on a common semiconductor substrate.

10. An EEPROM semiconductor device comprising:

(a) a plurality of field insulating films each extending perpendicularly to word lines;

(b) a plurality of memory cells arranged in a matrix, each memory cell including a floating gate, a control gate formed on said floating gate and doubling as a word line; and source and drain regions located at either sides of said control gate;

(c) a first bit line extending perpendicularly to said word lines and connecting drain regions of said memory cells with each other; and

(d) a first common source line extending in parallel with said word lines and connecting source regions of said memory cells with each other.

11. The EEPROM semiconductor device as set forth in claim 9, wherein said first bit line is constituted of a first metal wiring layer.

12. The EEPROM semiconductor device as set forth in claim 11, wherein said

first metal wiring layer is composed of aluminum.

13. The EEPROM semiconductor device as set forth in claim 10, wherein said first common source line is constituted of a second metal wiring layer.

14. The EEPROM semiconductor device as set forth in claim 13, wherein said second metal wiring layer is composed of aluminum.

15. The EEPROM semiconductor device as set forth in claim 10, further comprising a plurality of second common source lines formed above said source regions of said memory cells, and wherein said first common source line connects said second common source lines with one another.

16. The EEPROM semiconductor device as set forth in claim 15, wherein both said second common source lines and said bit line are constituted of a first metal wiring layer.

17. The EEPROM semiconductor device as set forth in claim 16, wherein said first metal wiring layer is composed of aluminum.

18. The EEPROM semiconductor device as set forth in claim 10, further comprising CMOS logic circuit including both said bit line and said first common source line, and formed on a common semiconductor substrate.

19. The EEPROM semiconductor device as set forth in claim 10, further comprising backing wiring layers each of which is connected to said word lines at every certain number of bits.

20. The EEPROM semiconductor device as set forth in claim 19, wherein

both said backing wiring layers and said first common source lines are constituted of a second metal wiring layer.

21. A method of fabricating an EEPROM semiconductor device, comprising the steps of:

(a) forming a plurality of field insulating films in parallel on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon layers in parallel with one another perpendicularly to word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said first polysilicon layer to thereby form a control gate and a floating gate;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

(h) forming a first metal wiring layer which is patterned so as to form both a common source line extending in parallel with said word lines and connecting source regions to one another, and an extended bit line connecting said drain region to a bit line;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

(j) forming a second metal wiring layer which is patterned so as to form a bit line connecting said drain regions to one another.

22. The method as set forth in claim 21, wherein said second gate insulating film has a three-layered structure of oxide/nitride/oxide films.

23. The method as set forth in claim 21, wherein said first and second metal wiring layers are composed of aluminum.

24. A method of fabricating an EEPROM semiconductor device, comprising the steps of:

(a) forming a plurality of field insulating films in parallel on a semiconductor substrate;

(b) forming a first gate insulating film in each of active regions;

(c) forming a plurality of first polysilicon layers in parallel with one another perpendicularly to word lines;

(d) forming a second gate insulating film and a second polysilicon layer all over the product resulting from said step (c);

(e) patterning said second polysilicon layer, said second gate insulating film, and said first polysilicon layer to thereby form a control gate and a floating gate;

(f) forming drain and source regions;

(g) forming a first interlayer insulating layer all over the product resulting from said step (f);

(h) forming a first metal wiring layer which is patterned so as to form both a bit line extending almost in parallel with said field insulating films and connecting drain regions to one another, and an extended common source line connecting said source region to a later mentioned common source line;

(i) forming a second interlayer insulating layer all over the product resulting from said step (h); and

(j) forming a second metal wiring layer which is patterned so as to form a common source line connecting said source regions to one another.

25. The method as set forth in claim 24, further comprising the step of forming backing wiring layers connecting to said control gate at a certain interval.

26. The method as set forth in claim 25, wherein said backing wiring layers are constituted of said second metal wiring layer.